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Hybrid Row Architecture Optimization for Sub-3nm Physical Design

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Abstract

As semiconductor technology is moving toward sub-3nm nodes, traditional design approaches are faced with enormous obstacles related to power, performance, and area (PPA) optimization; ensuring low interconnect delays; and integration of devices. Hybrid row architecture allows flexibility and scalability through the use of non-uniform standard cell layouts, heterogeneous devices, and innovative interconnect solutions. In this review, we examine new trends in hybrid row architectures and their potential for making contributions toward interconnect design-technology co-optimization, BEOL scaling, CFET integration, and 3D-IC realization. We also review how hybrid rows fit into the canon of other new design paradigms such as hierarchical graph embedding and machine learning based optimization. This review documents both the architectural advantages and practical implementations of hybrid rows with respect to enabling advanced physical design at sub-micron and likely nanoscale devices while still permitting (and perhaps enabling) integration of plasmonic and photonic devices for next generation computing systems.

Keywords: Hybrid Row Architecture; Sub-3nm Design; Design-Technology Co-Optimization; Advanced VLSI

1. Introduction

Moore's Law has sustained a pursuit of semiconductor technology to sub-3nm nodes where traditional scaling is challenged by power, performance, and area (PPA). Moreover, increased device density and quantum mechanical limitations, and parasitic effects will require new design methods. One method is hybrid row architecture optimization. Hybrid row architecture can provide mixed cell heights, transistors type, and interconnect topologies in standard cell rows that can provide additional flexibility and resource utilization at advanced process nodes.

As the semiconductor industry reaches the physical and economic limits of planar transistor scaling, device and interconnect co-optimization will be critical. This paper reviews the state-of-the-art methods and ideas of hybrid row architecture for sub-3nm, looking at recent advances in design-technology co-optimization (DTCO), back-end-of-line (BEOL) scaling, complementary FET (CFET), 3D integration, and unique benchmark approaches.

This study reviews how hybrid row arrangements of core fabric, because of their flexibility, can assist in alleviating PPA bottlenecks, minimise interconnect delays, and allow increased integration density. In addition, it considers how such arrangements work with other scaling enhancers and advanced physical design approaches to meet the needs of next-generation computing systems.

2. Challenges in Sub-3nm Physical Design

At the sub-3nm technology nodes, there are worsened interconnect delay and resistance-capacitance (RC) challenges as wire scaling becomes more aggressive with interconnects becoming larger compared to active gate areas.

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Interconnects are compromising overall performance, since some delays are worse than the worst gate delay. In addition, it introduces stability issues in power integrity and signal integrity challenges which need to be mitigated. The key mitigation approach lately is either to hold design, or use design-technology co-optimization. Hybrid rows allow design-technology co-optimization as it allows the interconnect device with local layout flexibility, design cell placement strategies, and mitigate the RC bottleneck. Recent optimization analysis study encouraged scaling boosters as a possible used relaxation; air gaps, semi-damascene metallization, self-aligned vias overall will enhance sub-3nm within interconnect scaling but will give diminishing results based on layouts and cell-level design alternatives where hybrid rows offer a major contribution [1].

Advanced nodes are also switching to new gate-all-around (GAA) transistors and not just FinFET, and in most cases are nanosheet FETs, giving layout complexity. Hybrid row architectures would allow different types and sizes of transistors in the same layout structure and keeping design to technology integration with design flexibility increase layout density and silicon area waste could be minimized. The PDN challenges are worse at advance nodes the power delivery network (PDN) becomes congested, using hybrid rows has allowed the opportunity to better distribute power grids via modular networks [1].

3. Emerging Methodologies in IC Physical Design

The growth of hybrid row architectures has benefited from growing interest in new approaches to integrated circuit (IC) physical design and methods of incorporating machine learning (ML) methodologies into design space exploration. As a recent example, the emerging community on ML in multi-level CAD (MLCAD) has situated intelligent algorithms for placement, routing, and power optimization in sub-3nm nodes as die-scale correlated opportunities in modern IC design. The hybrid row architecture has benefitted from these methods as it enables hierarchical optimizations at the level of the cell and the chip. The DATC (Design Automation Technical Committee) framework further establishes the ways that emerging design methodologies energetically leverage hybrid design techniques in order to better accommodate IC design work flows that are scalable and adaptable [2] .

Hybrid row optimization further improves placement density via the hybrid use of standard cell rows and custom cells that support better utilization of white space and reduces routing depth and congestion. This hybrid row optimization is particularly valuable in core portions of the design with lots of complex logic, and potentially around memory macros, since uniform cell rows could generate a sub-optimal, uniform layout. The configurable use of hybrid rows supports many design constraints and is an ideal fit for emergent EDA tools that will incorporate ML-style driven placement and routing engines. Each generation of design delivery will further inform the timing and choice of layout strategies that share specific design goals to potentially expediate better overall PPA [2].

4. BEOL Scaling and Hybrid Row Implications

Back-end-of-line (BEOL) scaling is a critical factor for developing sub-3nm technology, especially with applying scaling boosters to minimize RC parasitics. Upgraded ring oscillator (RO) analysis is allowing us to take advantage of hybrid row architectures and their local routing channels and non-standard via placements to potentially realize BEOL scaling boosters. The technologies of air gaps and dielectric material diversity can be realized clearly in hybrid row architectures, which can help improve speed and lower power dissipation [3].

Hybrid row designs also provide an improvement in thermal management as a result of enabling heterogeneous material integration that is important for sub-2nm nodes where BEOL scaling and thermal management are again very important, especially for high-performance computing (HPC) where thermal dissipation can limit operating frequency. Hybrid rows enable localized design approaches such as variable cell height and customized metal layers to accommodate optimal thermal profiles while allowing for performance enhancement [3].

Hybrid rows also allow for semi-damascene and subtractive metallization processes to support this route to reduced via resistance / capacitance. In some cases, these metallization processes require some layout adaptations or variations that can be supported through the modularization offered through hybrid architectures. This allows the use of custom metal pitches and via placements to achieve spatial improvements in performance (specifically interconnect performance) without compromising the regularity of the layout [3].

5. Device-Level Integration with Hybrid Rows

CFETs (complementary FETs) are an important device innovation relative to sub-3nm nodes, which make continued scaling possible beyond nanosheet FETs. Hybrid row architectures are natural candidates for CFET integration since they can fit the vertical stacking of n- and p-type transistors into a single footprint, allowing for greater logic density and higher drive current. However, CFETs also introduce new design and layout limitations, particularly with respect to gate alignment and contacts. Hybrid rows with their non-uniform architecture facilitate custom cell templates to effectively address the limitations of CFET designs [4].

In the same way, hybrid rows help CFET performance by allowing asymmetric designs, enabling an optimization of critical path delay and power. By allowing non-uniform cell sizes and different local interconnects, hybrid rows can take advantage of the benefits of CFETs without overly complex design. Hybrid rows also help facilitate DTCO strategies for CFETs since both device and interconnect layers can be co-optimized at a higher level of granularity [4].

In a standard cell library context, hybrid row architectures allow CFET-based cells and traditional GAA cells to coexist, enabling backwards compatibility and easier technology migration paths. This is particularly useful in technology transition periods where mixed-device designs are needed. Hybrid rows provide the design flexibility to support a heterogeneous cell library, integrating CFET-based cells and traditional GAA cells (while maintaining overall design and manufacturability considerations) [4].

6. Design Technology Pathfinding and Hybrid Rows

Frameworks like PROBE3.0 focus on pathfinding for design-technology at sub-3nm nodes because of the importance of hybrid row architecture. Pathfinding is the evaluation of design and technology alternatives for the best payoff for PPA. Hybrid rows enhance this type of pathfinding design because they offer a flexible layout canvas to evaluate different design options more efficiently. The modularity of hybrid rows allows for rapid prototyping and design iteration, which is crucial at the beginning of technology development [5].

Also, hybrid rows improve design enablements by allowing fast layout generation and allowing advanced designs rules to be combined. These can be double patterning, EUV lithography limitations, and density aware placement strategies. Hybrid rows allow flexible design structures, which enable adaptations without excessive overhead time. Also, hybrid rows allow for better yield optimization by allowing localized design rule enforcement which ensures lower defect density and more manufacturability [5].

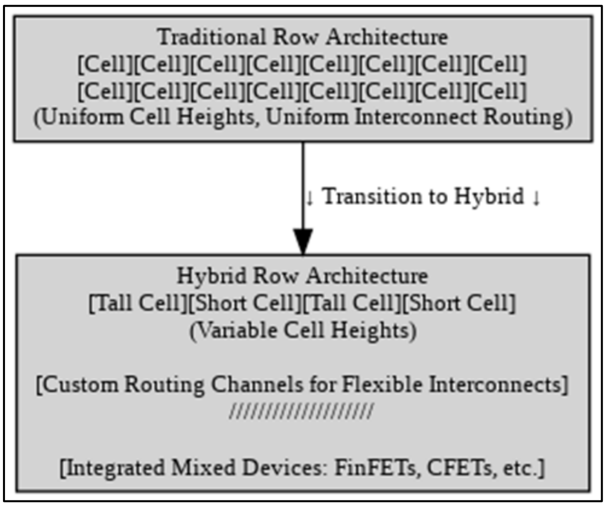

Figure 1 Schematic representation of traditional vs hybrid row architectures showing variable cell heights and interconnect flexibility (adapted from [5])

7. 3D Integration and Hybrid Row Relevance

Three-dimensional integrated circuits (3D-ICs) could be a key to solving challenges related to sub-3nm scaling. By placing dies vertically instead of side-by-side, 3D technology can avoid previous planar scaling limitations. The hybrid row architecture is critical in backend implementation of 3D-ICs; in particular, it will help with local interconnect congestion and through-silicon via (TSV) placement. The Open3DBench framework specifically targets this front with the evaluation of performance, power, and area (PPA) for 3D-ICs and show that the hybrid row architecture significantly enhances inter-die routing and mitigates thermal dissipation in 3D-IC layouts [6].

In the case of 3D-ICs, hybrid rows enable die-specific customizations that support different cell architectures in each tier. This style enables workload-specific optimization including if logic functionality, memory functionality or I/O functionality can be placed in different stacked die according to either locality of workload or purpose of die. Hybrid rows of heterogeneous dies accommodates the diverse placement and routing of a more efficient design with respect to PPA and performance at a system level [6].

Furthermore, hybrid row architectures can assist with controlling thermal gradients in a 3D stack through thermal aware place and localized power management techniques which play a crucial role in determining the design reliability and functional performance of thermally-stressed features expected from densely packed 3D systems. The facility to vary cell structure and interconnects at a local level gives hybrid rows great separation from a physical design perspective compared to more traditional methods applied to 3D-IC [6].

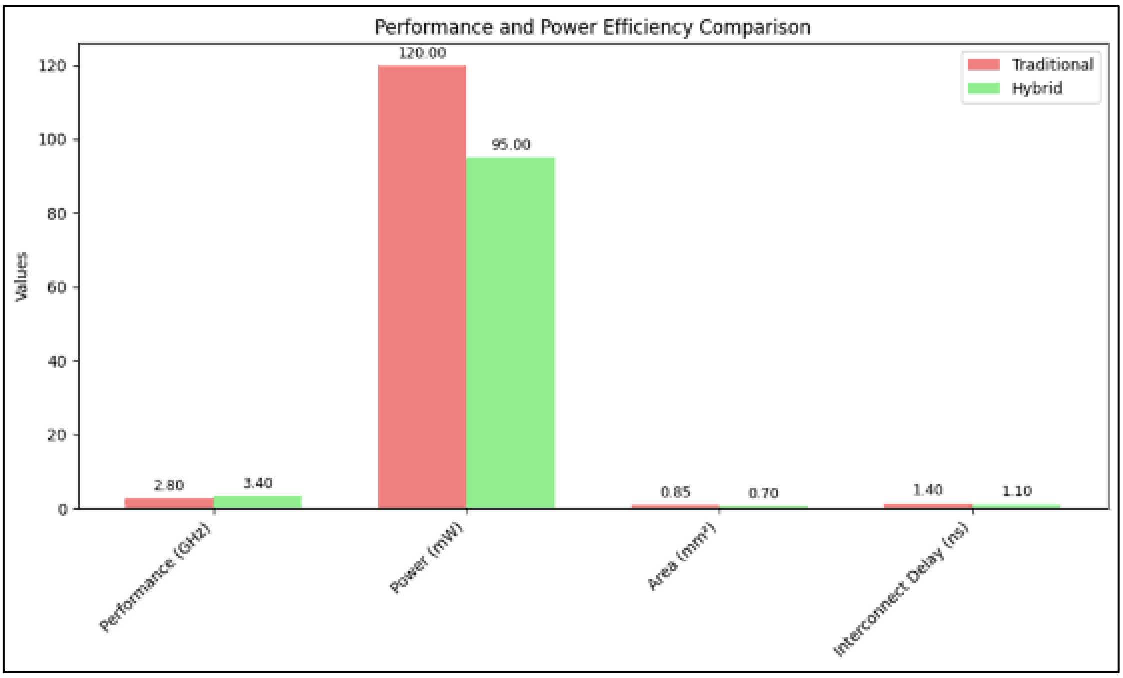

Figure 2 Comparative performance and power efficiency improvements achieved with hybrid row architecture in sub-3nm nodes (adapted from [6])

8. Research Infrastructure and Design Frameworks

Modern physical design processes require a strong research infrastructure, specifically for advanced VLSI technologies. Hybrid row architecture has profited from this notion through the support of advanced design tools and open-source frameworks. These recent studies have attracted attention to the considerations around scalable design flows and reliable process design kits (PDKs) that will accommodate hybrid layouts. These tools are necessary to execute hybrid rows in prototype designs and commercial products [7].

In addition, hybrid rows are in alignment with the Government and industry roadmaps on advanced packaging and heterogeneous integration. Hybrid rows offer one of consider the future of design as both packaging complexity is increasing and advanced interposer designs, as well as chiplet-based systems, are becoming more prevalent. This integration matters because it propels the journey for high bandwidth memory (HBM), photonic interconnects, and other advanced elements of packaging [8].

9. Hybrid Row Architecture in Plasmonic and Photonic Device Integration

As sub-3nm technology nodes extend the limits of classical electronics, the usefulness of integrating plasmonic and photonic devices into semiconductor platforms becomes paramount. The use of plasmonic and photonic devices can provide much faster data transfers, energy efficiency, and overall system improvements. However, integrating such devices poses serious physical design challenges due to material requirements, larger features, and sensitivity to alignment and interconnect structures. Hybrid row architecture will become an important part of such integration by taking advantage of layouts that can account for the electrical and physical limitations of the plasmonic and photonic elements [9].

The hybrid row structure allows for device placement in certain areas of the chip, while preserving the uniformity and density of typical logic cells. This allows the isolation of the important chips, reducing their cross-talk, and allowing for more optimized power delivery and thermal effects. Specifically, hybrid rows can be planned to reserve space and routing channels in accordance with the optical paths of photonic waveguides and the metallic patterns of plasmonic interconnects. The advantage of this modularity will allow for the added advantages of new optical devices without impinging upon the fabric of the digital design [9].

Furthermore, hybrid rows can implement co-design philosophy with plasmonic devices optimized in conjunction with electronic circuits of the nodes. Co-design is critical for fully realizing the benefits of optical interconnects in high-performance computing systems. Hybrid row architecture allows custom placement strategies and combinations for electronic and photonic devices, paving the way for new computing paradigms that integrate the speed of optics with the flexibility of electronics [9].

9.1. Fast Design Technology Co-Optimization Using Graph Embedding

The growing complexity that comes with sub-3nm designs will necessitate advanced design technology co-optimization (DTCO) frameworks that can work fast and efficiently. Hybrid row architecture is highly suited for such frameworks, especially when utilizing hierarchical graph embedding methods involving hierarchical graphs. The purpose of this approach is to capture and represent the abstract structures that comprise a design so effective placement, routing and build strategies can be discovered for the best layout. The unique hierarchical non-uniform placement of hybrid rows adheres closely with graphs used to model connectivity, timing and all physical connectivity between the various layers of the design [10].

Graph embedding approaches allow for the even faster exploration of hybrid row configurations by concurrently using both embedded cell properties and embedded interconnect properties in a multi-dimensional design space. This means designers can analyse performance, power and area trade offs in real time and through an iterative process, redefine their layout strategies for the better. The hierarchical graph also has the advantage of being able to map the significant complexities often found in modern designs to smaller subgraph localised regions contained within hybrid rows. This allows the work to be parallelizable and ultimately streamline the design cycle that is much needed during rapid turn around product development cycles [10].

In addition, the co-optimization frameworks will facilitate machine learning algorithms that can predict the effects of a variety of hybrid row configurations on PPA metrics. Following the physical design tools will allow these models to improve their predictions in a feedback loop, ultimately yielding very optimized hybrid row solutions. This approach is vital for dealing with increased variability and uncertainty with advanced manufacturing processes at sub-3nm nodes [10].

Table 1 Comparative analysis of traditional vs hybrid row architectures in sub-3nm physical design (compiled from [1]–[10])

Feature	Traditional Row Architecture	Hybrid Row Architecture
Cell Height Uniformity	Fixed	Variable (mix of multiple heights)
Interconnect Flexibility	Limited	High
Device Type Integration	Homogeneous	Heterogeneous (FinFET, CFET, etc.)
Routing Congestion	High in dense areas	Reduced through modular layout
Thermal Management	Uniform strategy	Localized strategies

Advanced Packaging Support	Limited	High (Chiplet, 3D-IC, etc.)
Compatibility with Emerging Devices	Poor	Excellent (Plasmonic, Photonic, etc.)
Design Optimization Time	Longer	Shorter with ML and co-optimization tools

10. Conclusion

In the field of semiconductor design, optimizing hybrid row architectures for sub-3nm nodes will undoubtedly become a vital research area going forward. There is an observable trend in the engineering community, regarding the move towards heterogeneous integration and design at system-level optimization. Hybrid row designs will serve as a flexible and scalable physical design strategy as the ingenuity of engineers advances. Newer devices such as CFETs, 2D materials, and quantum dots will require unique layout strategies, of which hybrid rows will facilitate.

The ongoing enhancement of design automation with strategies that utilize AI optimization, hierarchical modeling, and real-time feedback is necessary to fully leverage hybrid row architecture. In addition, it will require collaboration between device engineers, interconnect specialists, and EDA developers to address the challenges of design at sub-3nm. As hybrid rows link each discipline together, they provide a comprehensive approach to design and manufacturing co-optimization.

Also, standardization of hybrid row templates and open-source design frameworks can help make wide-spread use possible in the industry. Initiatives like Open3DBench are also useful for developing open benchmarks, and for examining and improving hybrid row approaches in different usages and technology nodes. The semiconductor industry is on the brink of the beyond-silicon computing era, and it is important that hybrid row technology evolves with the industry.

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